# Hybrid III–V/Silicon Nanowires

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**Abstract**

Semiconducting nanowires are emerging as a route to combine heavily mismatched materials. The nanowire dimensions facilitate the defect-free integration of the two most powerful semiconductor classes, group IVs and group III-Vs. These combinations may enhance the performance of existing device concepts, and also create new applications. In this chapter we review the recent progress in heteroepitaxial growth of III-V andIVmaterials. We highlight the advantage of using the small nanowire dimensions to facilitate accommodation of the lattice strain at the surface of the structures. Another advantage of the nanowire system is that anti phase boundaries are not formed, as there is only one nucleation site per wire. In this chapter, we will discuss three different heteroepitaxial III-V/Si morphologies, III-V nanowires on group IV substrates, and axial and radial heterojunctions. Advanced analysis techniques are used tocharacterise the quality of the heterointerfaces. Finally, we address potential applications of III-V/Si nanowires.

**Introduction**

The success of the semiconductor industry originates from the abilityto precisely tunethe electronic properties of semiconductor materials. Different approaches are used to enhance the functionality of semiconductors, such as impurity doping, alloying, heterostructuring, and straining. All these methods are based on the addition of chemical elementsto a pure semiconductor. An important example is the invention of the GaAs/AlGaAs heterostructure, which has enabled the development of the laser diode and the high electron mobility transistor (HEMT).In this chapter we will discuss the combination of 2 different classes of semiconductors, group IV, like Si and Ge, and group III-V, like GaAs and InP. We will focus on a relatively new materials system, *i.e* nanowires (NWs), in which strain can be effectively relieved at the surface due to the small dimensions, therefore relaxing the requirements on lattice matching.This system thus offers enhanced flexibility over the conventional layered structures in combining different semiconductor materials. These new combinations may boost the performance of already widely explored device concepts, such as transistors and solar cells, but may also open new applications, such as in quantum information technology. After a discussion on the different challenges related to the combination of Si and III-V semiconductors, we will discuss the growth of III-V nanowires on group IV substrates[123456789], and then focus on the growth of heterostructures within nanowires in the radial[1415] and axial[10111213]directions (Figure 1).

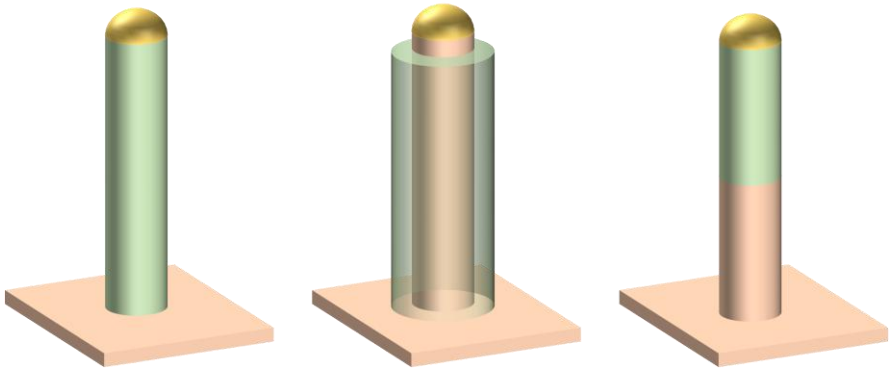

**Figure 1:** Schematic of the different Si/III-V nanowire geometries: III-V nanowire on Si, III-V/Si core-shell nanowire and III-V/Si axial nanowire.

**Challenges in epitaxial Si/III-V interfaces**

Silicon is the material platform of microelectronics. Single crystalline Si wafers, up to 450 mm in diameter, offer a low cost substrate for advanced electronic and micromechanical components. Silicon has a high thermal conductivity, is mechanically robust, and has a stable oxide. However, silicon has an indirect bandgap (at 1.1 eV) and therefore it does not efficiently emit light. This significantly limits the applications of silicon in photonic technology. Its isotope $^{28}$Si has zero nuclear spin which is particularly attractive for quantum information technology, where a single electron spin must be isolated from other spins to be used as a quantum bit.

In contrast, most III-V semiconductors have a direct bandgap and therefore are perfectly suited for optoelectronic devices such as light-emitting diodes (LEDs) and solid-state lasers. Importantly, solar cells of the highest efficiency are made of III-V semiconductors because of the high light absorption. Some III-V's, especially those based on the heavier elements, such as indium antimonide, exhibit extremely high electron mobility,and very strong spin-orbit interaction, enabling fundamental breakthroughs in quantum science and technology such as NW spin-orbit quantum bits (qubits) and Majorana fermions.[16] Importantly, the electronic properties, such as the band gap energy and the carrier mobility, of III-V semiconductors can be tuned by varying the chemical composition (*e.g.* by alloying to form ternary or even quaternary compounds such as $In_xGa_{1-x}As_ySb_{1-y}$). However, III-V semiconductors have poor mechanical integrity (they are fragile) and some of the constituents are in short supply, like indium, which makes them expensive. For a number of important applications that will be discussed here it is valuable to combine the best properties of Si and III-V semiconductors, but the success depends on the quality of heterojunctions between the two semiconductor classes.

'Epitaxy' is derived from the Greek word meaning "ordered upon" and is the crystalline deposition of material on a substrate with identical lattice structure and orientation. For heteroepitaxial growth, materials with different lattice parameters are combined. If the lattice mismatch between the deposited film and the substrate is large, typically a few percent, misfit dislocations can be incorporated near the interface. Alternatively, add layers may form three-dimensional nuclei to release the strain in order to minimize the energy in the system, at the cost of creating more surface. The heterostructure growth method that Kroemer and Alferov used was to stack two-dimensional layers of

atoms using materials of similar lattice constant and surface energies (to favour layer-by-layer growth rather than island growth) by Molecular Beam Epitaxy (MBE). This growth technique made it possible to produce defect-free bulk GaAs/$Al_xGa_{1-x}As$ heterojunctions. In contrast, semiconductors with higher lattice mismatch suffer from the creation of threading dislocations, which release the strain accumulated during the formation of a new material layer. Dislocations and crystalline defects are the main challenge in crystal growth. They trap carriers and behave as recombination centers for photons, which makes them harmful for device performance and limits practical semiconductor combinations in bulk two-dimensional heterostructures.

In addition to strain, defect formation at the heterointerface can be caused by differences in polarity of the two semiconductors, as is the case for instance for silicon and gallium phosphide (a group IV/III-V interface). The essence of the problem is that GaP can nucleate on Si by either forming Si-P or Si-Ga bonds. Any non-uniformity during growth can lead to the formation of nuclei having opposite polarities, and when these nuclei merge a so-called antiphase boundary(APB) is formed. An APB is a planar defect, in which the regular atomic ordering is interrupted; at the boundary the atomic ordering is for instance 'Ga-P-P-Ga' instead of the regular 'Ga-P-Ga-P'. Importantly, when the surface is uniformly covered with one of the precursor elements, APBs can still be formed at monoatomic steps on the substrate surface. Along with twins and dislocations APBs are a major limitation that specifically reduces the potential of structures that combine Si with III-V semiconductors in the bulk.

Nanowires are one-dimensional crystals with a large aspect ratio. They have a diameter of several nanometers and their length can vary from a few micrometers to several millimeters. From a materials engineering point of view, the very small cross section of NWs is highly advantageous because strain can be elastically released at the interface between semiconductors with large lattice mismatch. Rather than producing crystalline defects, the atoms adjust their spacing to minimize strain because they are free to expand towards the sidewalls of a NW. Moreover, as it will be described below, nanowires grow via a layer by layer mechanism which involves a single nucleus per layer. There are therefore no anti phase boundaries in nanowires. Thanks to their ability to accommodate strain and the absence of APB, nanowires are therefore perfect candidates for III-V/Si heterostructures.

**III-V nanowires on Si substrates**

III-V nanowirescan be grown on Si substrates by using different growth mechanisms, such as selective area growth[17,18] or by the vapor-liquid-solid (VLS) method.Nanowires grown by the VLS mechanism are nucleated from a nanometer sized metal seed or catalyst particle that collects the precursor material from the vapour phase, establishing a local supersaturation. There are a few examples showing that the metal particle acts as a catalyst for the decomposition of the precursor molecules.[19,20] A vapour pressure of the precursor components can be created by means of molecular beam epitaxy (MBE), metal organic vapour phase epitaxy (MOVPE) and related techniques, pulsed laser ablationor by simple evaporation of the precursor material.

When the supersaturation has been reached, crystalline material precipitates underneath the metal particle. In order to enable epitaxial growth of a nanowire it is of crucial importance to have a clean and crystalline substrate surface. Methods to clean Si substrates are well established and an etching step with hydrofluoric acid is mostly included. The catalytic metal particles are deposited directly after substrate cleaning. So far, Au has mainly been used as the active particle, but also alternative metals,oxides and silicides, being compatible to standard silicon processing, have been used. Importantly, any exposure to air affects the epitaxy, since Au catalyzes the oxidation of Si and tens of nm thick $SiO_2$ layer forms on top of the Au particle within days already at room temperature[21].

Another method to grow one-dimensional structures is by using selective area growth (SAG). Holes are defined in an amorphous dielectric layer, which cover on epitaxial substrate. Taking into account that growth only takes place from the opened areas pillar structures will be formed. Since no catalyst particle is used with this method, no impurity atoms from the catalyst will be incorporated in the semiconductor material. Another advantage is that the III-V / Si wire/substrate heterointerface will not be affected by alloying of the catalyst particle with the substrate.Such strategy was extended to InAs nanowires selectively grown in vertical $SiO_2$ nanotube templates fabricated on Si substrates. After removal of the template, the InAs nanowires show an epitaxial relationship with Si and are single-crystalline. Misfit dislocations are however present at the InAs/Si interface. (REF)

Scanning electron microscopy (SEM) can give a first indication of nanowire epitaxy. Epitaxial growth results in alignment of the nanowires in specific directions determined by the crystal symmetry of the substrate. However, orientation of one-dimensional structures

can also be obtained during growth by other mechanisms, such as interaction with external fields[22] or with a gas flow[2324]In general, the III-V wires tend to grow in the [111]B direction,[2526]and vertical growth can be induced on [111]B-oriented III-V substrates. We should note however that the elemental semiconductors, such as silicon, are not polar, and all {111} facets are chemically equivalent. This means that the III-V wires can grow in the four <111> directions on a [111] oriented Si substrate;one orientation perpendicular to the surface and three orientations having a 19° angle with the surface, and in-plane components at 120° from each other.This has, for instance, been observed for the growth of InP on (111) oriented silicon substrates[3] having a mismatch of 8.1% There are three clearly noticeable orientations with in-plane components parallel to the sides of an equilateral triangle. Some wires are oriented perpendicular to the surface, and in this top view they appear as small bright spots.

It is possible to terminate a group IV substrate by either a group III or group V element using surface reconstructions as has been shown by Fukui[6]using selective area growth. In this way a quasi-polar surface can be formed. This approach has been successful in obtaining high yield of vertically oriented III-V nanowires on (111) Si substrates. The scanning electron microscopy (SEM) image in Figure 1a shows the high yield obtained with this method.

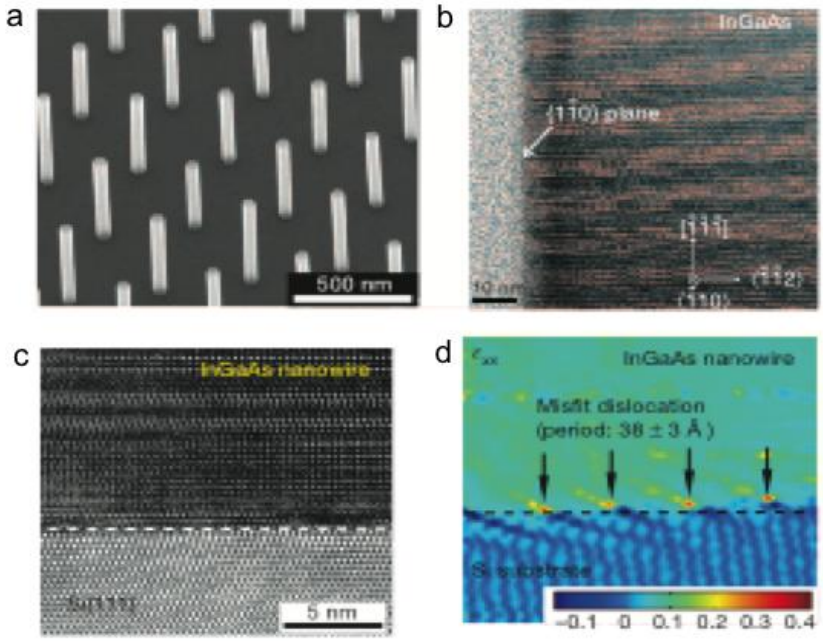


**Figure 1.**a) SEM image of InGaAs nanowires grown on a Si(111) substrate by using selective area growth (SAG). b) TEM image of a InGaAs showing the crystal structure and the

planar stacking faults. c) HRTEM image of the InGaAs wire/ Si substrate interface. d) Strain map obtained from the image in c) showing the periodic misfit dislocations.

The crystallographic relation between the substrate and an ensemble of nanowires can be substantiated by XRD (X-ray diffraction) pole figure measurements.[531] To record a pole figure, the detector is set at a $2\theta$ angle corresponding to one of the lattice spacings, and the substrate is rotated continuously around $\varphi$, and stepped around $\psi$. Pole figures are measured for the (111) reflections of the substrate and the wires.In the reference pattern of the silicon substrate, plotted in Figure 2c, (111)-spacings were found at four orientations typical for a (111)-oriented single crystal (these orientations are reflected by the wire orientations as observed with SEM). One set of reflections is in the centre of the pole figure, corresponding to the substrate normal, and three sets with $\psi$=19° and the in-plane angle of 120° with respect to each other.The pole figure for InP wires grown by MOVPE on Si(111) is shown in Figure 2c. The signals associated with the majority of the InP wires, labelled A (*i.e.,* about two-thirds of the total signal), matches the pole pattern of the substrate, providing an unambiguous signature of heteroepitaxial growth. With such pole figures the epitaxial relation between a range of III-V nanowires, such as GaAs, InP, and InAs, with the Si(111) substrate has been confirmed.[3] The difference in lattice spacings for the GaP/Si system was too small to be resolved in the pole figures.

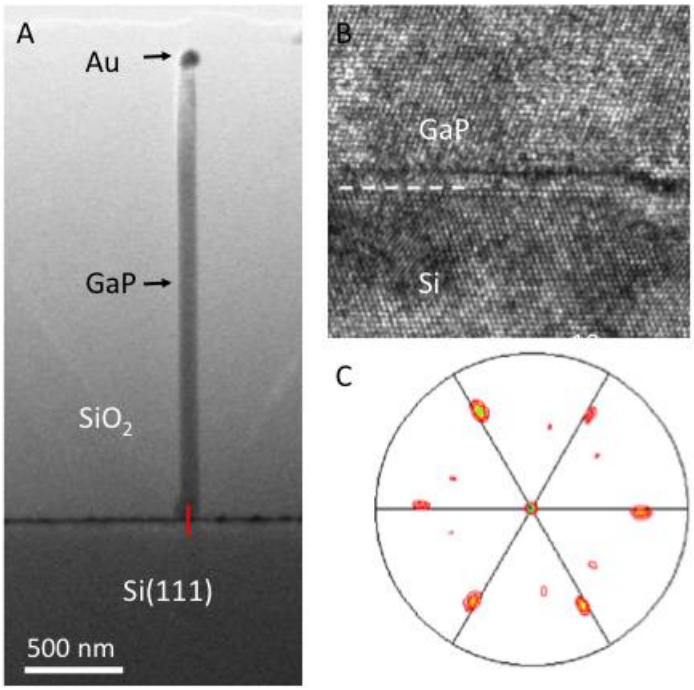

**Figure 2.**a) Cross sectional TEM image of a GaP nanowire grown on a Si(111) substrate by using the VLS mechanism. b) HRTEM image of the GaP/Si interface showing the roughness, which is induced by alloying of the catalyst particle with the Si substrate prior to growth. c) Pole figure of InP wires grown on Si(111).The three-fold symmetry demonstrates the epitaxial growth. The three other intense peak show that there are twin planes present in the nanowires.

The wire/substrate interface of individual wires can be studied in great detail by transmission electron microscopy (TEM). For this study, vertical cross sections were sliced with a focused ion beam (FIB) and thinned by argon ion milling. To provide mechanical support during this process, the wires were embedded in a microns-thick silicon oxidelayer, deposited by spin-on process or by plasma-enhanced chemical vapor deposition (PECVD). Figure 2a shows an overview of a cross-sectional TEM image of a GaP wire grown on a Si(111) substrate. In Figure 2b the wire/substrate interface was imaged at high-resolution. The lattice planes continue from the substrate into the nanowire showing the epitaxial relation.It can also been seen that the substrate wire interface is not flat. This is probably due to alloying of the Au catalyst particle with Si from the substrate roughening the surface.

Such alloying can be avoided by using selective area growth. In Figure 1c the flat heterointerface between InGaAs/Si has been imaged at high resolution[27]. The heterointerface was apparently free of threading dislocations and antiphase boundaries, but had periodical misfit dislocations (see Figure 1d), indicating that the lattice mismatch has been plastically relaxed. These dislocation networks were formed only at the heterointerface. However, from TEM imaging it is also clear that these wires grown by SAG contain many planar stacking faults (Figure 1b). Recently, defect-free wurtzite InP wires have beengrown by SAG on corresponding substrates at very high temperatures, which exhibit very high optical quality.

III-V nanowires grown on Si have been explored for many different device applications. Recently, high quality field effect transistors (FET) have been demonstrated exploiting the high electron mobility of the III-V material and the vertical wire geometry to form a gate-around structure as shown in Figure 3a[27]. The gate around structure minimizes short channel effects such as drain-induced barrier lowering (DIBL) as is clear from Figure 3b. The III-V/SI heterointerface also allows improving alternative FET principles, such as the

tunnel-FET[28(REF)].Less power is needed to switch a tunnel FET compared to a 'normal' FET. By using heterostructures there is more freedom in tuning the band alignments between the different semiconductors and with this the performance can be optimized. Epitaxial integration of III-V with silicon also introduces direct band gap semiconductors into electronics. Various opto-electronic applications have been studied including LEDs, lasers and photovoltaic cells. Considering the optical quality of state-of-the-art nanowires it can be expected that this approach will result in devices, which can be competitive with standard III-V technologies, but then epitaxially integrated in silicon.

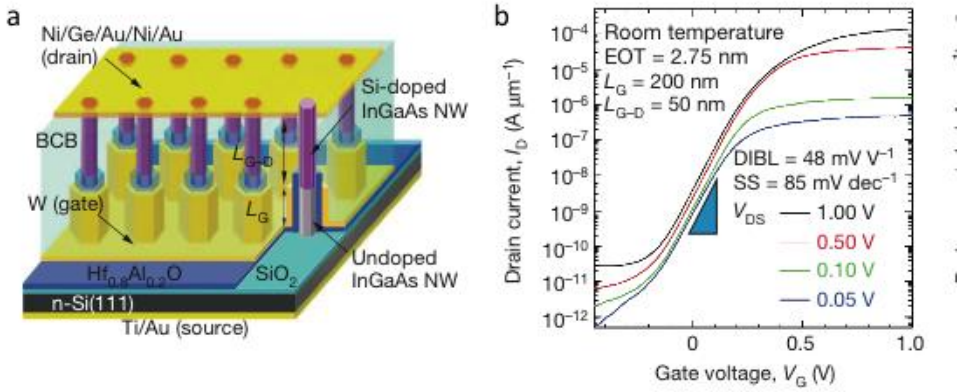


**Figure 3.** a) Schematic image of a field-effect transistor device based on an array of vertical InGaAs nanowire grown on Si(111). Note that the gate is all-around the nanowire channels. b) trans conductance characteristics of the device in a), showing good performance.

**III-V/IV radial core-shell nanowires**

A number of significant steps in the controlled synthesis of core/shell nanowire heterostructures have been recently achieved by various groups. In this review, we illustrate some of these results in the cases in which core and shell of the nanowire are grown using materials of the groups III-V and IV, as we did in the previous section. To begin with, *Algra et al.* (2011)[14] were able to synthetize the first III-V/IV core-shell system consisting of the combination of GaP and Si semiconductor materials. This group reported a method for transferring the desired crystalline structure from a GaP nanowire to the Si shell. Interestingly, such approach allows tailoring the crystalline structure of the shell material by suitably growing the core material in specific crystalline phases.

In their work, the growth of the GaP nanowires was performed using a metal-vapour phase epitaxy (MOVPE) reactor using trimethylgallium (TMGa) and phosphine ($PH_3$) as precursors by adding diethylzinc to the gas phase during growth. In particular, a designed twinning superlattice in zinc blende crystal structure present in the GaP nanowires was epitaxially transferred to the Si shell at 550 °C using $SiH_6$ as a precursor with a partial pressure of $3.4\times10^{-3}$ mbar. This important property allows designing new materials, like hexagonal silicon, which are more difficult to achieve in other systems, opening the path to a number of important applications.

*Conesa-Boj et al.* synthesized GaAs/Si core-shell nanowires by combining molecular beam epitaxy (MBE) and plasma enhanced chemical vapour deposition (PECVD)[29]. The GaAs nanowires were first grown in an ultra-high vacuum MBE chamber. After that, the wafers containing the original GaAs nanowires were transferred to the PECVD system. Before the deposition of the Si the wafers were subjected to a $H_2$ plasma treatment in order to reduce the oxide present on the sidewalls of the GaAs nanowires. By adjusting the concentration of silane radicals and reactive radicals in the plasma determine the nature of the Si shell.

In figure 4(a) and 4(b) two representative GaAs/Si and GaP/Si nanowires are shown. It is remarkable that in this growth approach the shell adopts the same crystalline structure as the core material, in these two cases in particular Si adopts the cubic and the hexagonal crystalline phases respectively. The insets in figure 4 also show the energy dispersive-X ray spectroscopy (EDX) compositional maps that illustrate the presence of the GaAs/Si and GaP/Si core-shell heterostructures, respectively.

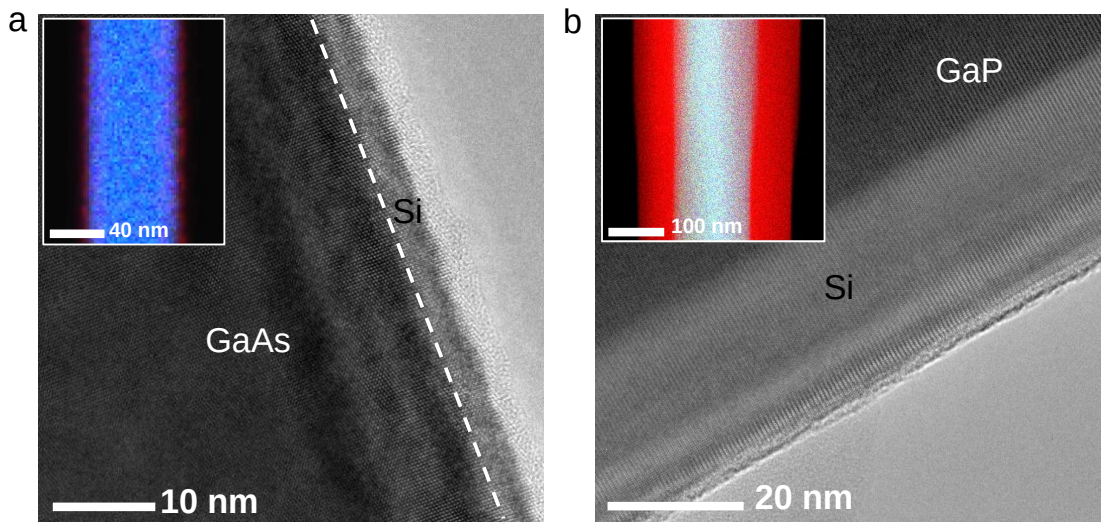


**Figure 4.** (a) and (b) high-resolution TEM images of a representative GaAs/Si and GaP/Si core/shell nanowires respectively. The insets correspond to the EDX compositional map confirming the presence of the GaAs/Si and GaP/Si core-shell heterostructures. In these maps Si signal is marked in red.

The structural quality of the junction in core-shell nanowires is one of the essential requirements that must be satisfied in order to implement such nanostructures in realistic nanodevices. It has been extensively demonstrated that one of the main sources of defect formation in core-shell systems is due to the lattice mismatch between the shell and the core leading to the appearance of misfit dislocations at the core and the shell interface. However, both experimental studies and theoretical models of defect formation have been mostly restricted to mismatched materials, where the appearance of defects is driven mostly by the difference in geometry and crystalline structure of the core and the shell.

As an illustration of the potentialities of structural characterization in core-shell systems, *Conesa-Boj etal.*[30]combined high-resolution transmission electron microscopy (HRTEM) with geometrical phase analysis (GPA) and finite element methods to determine and quantify the origin of the lattice distortion in GaAs/Si core-shell nanowires. The presence ofedge dislocations in such system produces a localized elastic distortion, in particular a tensile line crossing the diameter of the nanowire, which turns out to be around 4%, see the strain map along the axial directionshown in figure 5(a).

As a useful baseline to understand the essential features of the strain field observed experimentally, and to identify the three-dimensional structure of the defect, finite element (FE) simulations were performed. In particular the effects of an edge dislocation loop were simulated, assuming the dislocation loop lying in the (1-11) plane at the core-shell interface with Burgers vector b=a/3[1-11], as described the sketched in figure 5(b). Given that the FE simulation results were in agreement with the experimental results, this study suggested that the two edge dislocations observed in the GPA image are the fingerprints of an edge dislocation loop traveling around the nanowire core at the GaAs/Si interface and that the localized tensile strain is induced by a looplike dislocation configuration.

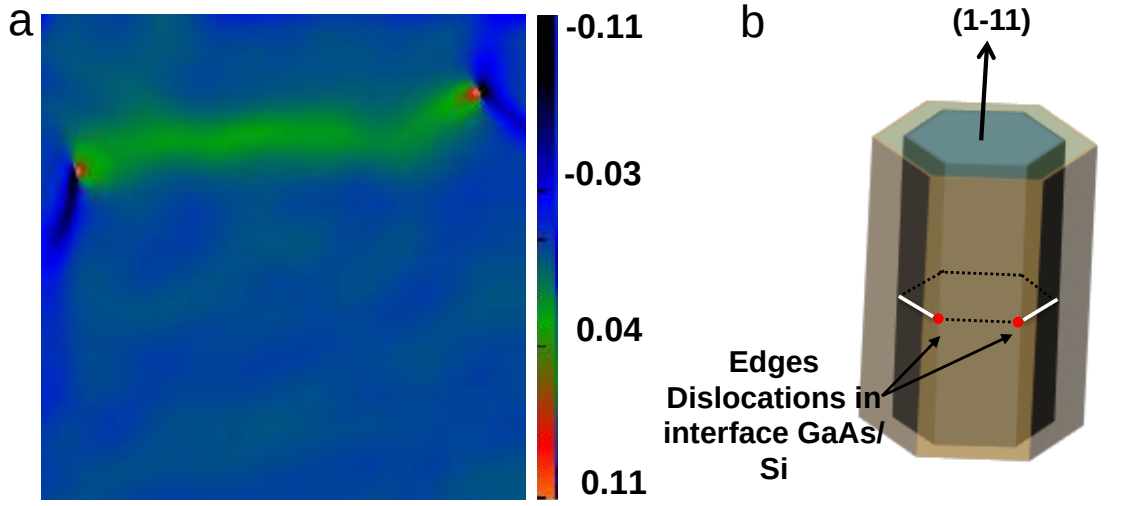


**Figure 5.** (a) Strain field map, where a tensile region crossing the nanowire diameter is visible (green line) and (b) Sketch of the nanowire assuming an edge dislocation loop , lying in a (1$\bar{1}$1) plane at the core–shell interface with Burgers vector b = a/3[1$\bar{1}$1].

In addition to highly mismatched materials, defect formation can also be ubiquitous when combining materials with similar lattice parameters. In these cases, the mechanisms of defect formation can be tightly related to specific growth process. This phenomenon has been explored for instance in the work of *S. Conesa-Boj et al.*[15], who reported it for GaP/Si core-shell nanowires. Despite the similar lattice parameters, the presence of defects, in particular "crack" defects, was observed. The crack defect can be modelled as a local fracture, that is, a region where the separation between two adjacent atomic layers is increased, as shown in Figure 6.

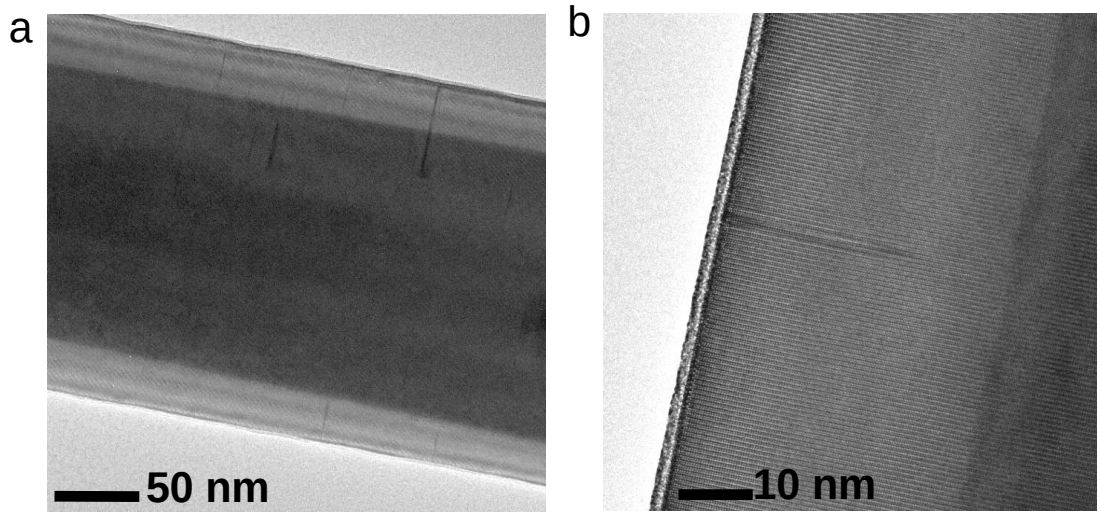


**Figure 6.** (a) Low-magnification TEM image of a GaP/Si core-shell nanowire, where the stripes with different contrast indicate the presence of cracks defects; (b) high-resolution TEM image of a lateral of a GaP/Si core-shell nanowire exhibiting a crack defect in the Si shell.

In order to reduce the formation of these types of defects, it is important to understand how their appearance is related to the details of the growth processes. In this case, it has been reported in the literature that the formation of such defects and their development into other type of defects is dependent on the brittle to ductile transition (BDT) behaviour. In the work we are discussing, different temperatures for the Si shell deposition were tested.

The main point to understand the mechanism for crack formation was that during Si shell deposition two different steps in terms of temperature were used. The temperature difference was enough to induce local changes of the dilatation coefficient in the crystalline structure of the Si shell and thereby allowing the formation of cracks and other kind of defects such as stacking faults and Frank-type dislocations. Such studies have lead to propose an alternative growth strategy to achieve defect-free hexagonal Si.

**Axial III-V/IV nanowire heterostructures**

Most of axial nanowire heterostructures realized so far involve different materials with the same crystal structure or the same material with different crystal structures. Multi-family semiconductor heterostructures involving different materials with different structures

started to appear only recently, increasing material combinations possibilities. Such novel material combinations implicate lattice mismatches ranging from almost 0% up to 10%, adding complexity to the system. Increasing mismatches lead to dramatic consequences in two dimensional heterostructures when plastic relaxation causes misfit dislocations. F. Glas[31] studied the effect of the stress relaxation on axial structures regardless of their chemistry. He theoretically observed that the critical thickness increases with the reduction of the nanowire heterostructure diameter. In other words, the nanowire geometry favours elastic relaxation and allows the combination of materials of large lattice mismatch in contrast with two dimensional heterostructures. In the particular case of Si/III-V heterostructures, geometrical parameters exist in which crystal defects due to strain relaxation do not appear, therefore it is theoretically possible to create misfit dislocation free Si/III-V axial heterostructures. However, the nature of each semiconductor is a major hindrance to axial Si/III-V's, in particular their chemical bonds and surface energy which have a direct influence on the growth mechanisms.

The first experiments on axial Si and III-V combinations were presented by *Dick et al* in 2007[10]. They focused their investigations on Si/GaP, GaP/Si, GaAs/Si and Si/GaAs heterostructure nanowires. The nanowires were grown by MOCVD using standard growth parameters for the respective segments. A purging step under $H_2$ of several minutes was used to remove precursors from the gas phase. This step also allowed to increase/decrease the growth temperature for the next segment. Straight segment were found for Si/GaP and Si/GaAs axial nanowires whereas the reverse stacking showed kinks. A thermodynamic model was developed and suggested that in analogy to 2D growth, the nanowires morphology (straight or kinked) strongly depends on the relative surface energies between materials.

Later in 2012, *Hocevar et al.*[11] published a complete work on multiple axial GaP/Si nanowires. The nanowires were grown in a MOCVD reactor at a constant temperature of 540°C. A growth interruption step was used between GaP and Si growth sequences. After the GaP segment growth, the group V source was shut down for several seconds, keeping the group III source on. The group III source was then shut down while the Si source was opened to grow the Si segment.

When no growth interrupt was performed between the GaP segment and Si growth sequences, all of the Si segments kinked at the GaP/Si interface. The authors suggested that

phosphorous atoms prevent Si entering the gold catalyst. As a consequence, Si doesn't uniformly alloy with the liquid gold particle and three-dimensional growth occurs. In contrast, when a growth interrupt takes place between GaP and Si growth sequences, all the Si segments are straight at the GaP/Si interface (Figure 7a). Phosphorous atoms are removed from the surface of the gold either by desorption or by the Ga atoms to form GaP. Consequently, Si absorbs uniformly on the Au surface, which results in a uniform Si concentration throughout the droplet, and layer-by-layer growth occurs.

By engineering the growth interrupts between growth sequences, Hocevar *et al.*[11]achieved Si/GaP (Figure 7b and 8) and multiple GaP/Si heterostructures along the nanowire axis. These nanowires exhibit interesting feature: (1) both materials grow from a AuGa alloy and (2) the nanowires diameter is smaller along the Si segment diameter than along the GaP segment. This diameter variation is mainly explained by the difference in contact angles (and therefore surface energies) between the AuGa liquid on a GaP surface and on a Si surface.

Inspired by the GaP/Si heterostructures, Hocevar et al integrated an optical emitter, a GaAs segment between GaP barriers along a Si nanowire. The GaAs segments emitted at 1.495 eV with photexcited carrier lifetimes over 1 ns, demonstrating a high crystal quality.

*Hillerich et al.*[32] grew axial GaP/Si and GaAs/Ge nanowires using various equipments such as MOCVD, CVD and in-situ UHV TEM. Between two growth sequences (between GaP and Si for example), the samples were cooled down to room temperature. High crystalline quality GaP/Si and GaAs/Ge segments were grown and crystalline defects formation some distance after the interface was investigated. From these experiments, it appeared that the droplet geometry drives the growth morphology: if the mismatch between the droplet diameter and the nanowire diameter is too high, crystal defects form in the newly grown segment. Therefore, by optimizing the growth parameters to minimize the gold droplet diameter change during the new growth sequence, straight GaP/Si and GaAs/Ge nanowire heterojunctions can be grown. Another strategy to create defect free III-V/Si nanowires proposed by *Hillerich et al*.[32]is to use an interlayer. They demonstrated that the use of Ge layers between GaAs and Si allowed the creation of defect free hybrid GaAs/Si nanowire heterostuctures. *Conesa-Boj et al*[29] achieved axial Si/GaAs heterostructures using a gallium-catalyzed VLS mechanism with a combination of MBE and PECVD techniques. They showed crystalline axial growth of Si on GaAs at 250 C substrate temperature and low silane flow

(Figure 9). This preliminary work is a major step forward as gold-free nanowires have strong potential for future integration of nanowires in CMOS technology.

*Prucnal et al*.[33] developed a route to create Si/InAs heterostructure nanowires using a combination of sequential ion beam implantation and flash lamp annealing. First Si nanowires were grown by Au-catalyzed VLS mechanism using a low pressure CVD system. The nanowires were then implanted at selected positions with As and In ions with a fluences of the order of $10^{16}$ ions/cm$^2$ for each element. The chosen ion implantation energies for In+ and As+ allowed the depth distribution of In and As atoms to overlap within the Si nanowires. The samples were annealed with a flash lamp annealing system to recrystallize the nanowires. The obtained InAs quantum dot/Si nanowires showed atomically sharp interfaces between Si and zinc blende InAs segments.

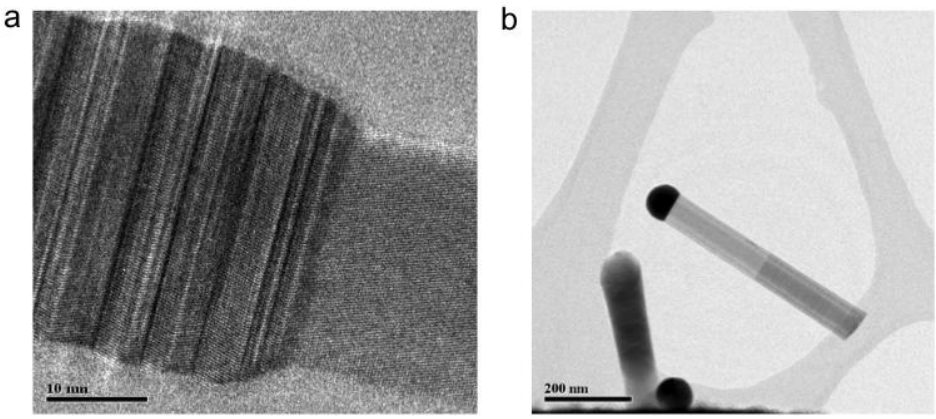


**Figure 7.** a) TEM image of GaP on Si heterostructure nanowire grown by Au-assisted VLS. B) TEM image of Si on GaP heterostructure nanowire grown by Au-assisted VLS.

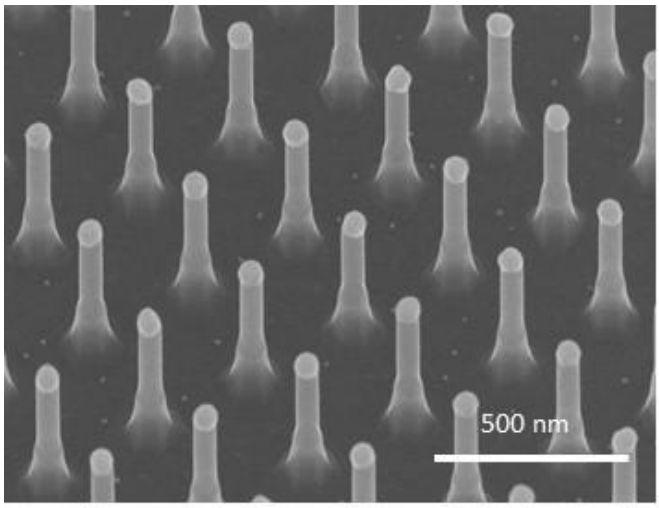

**Figure 8.** SEM image of an array of Si on GaP heterostructure nanowires grown by Au-assisted VLS.

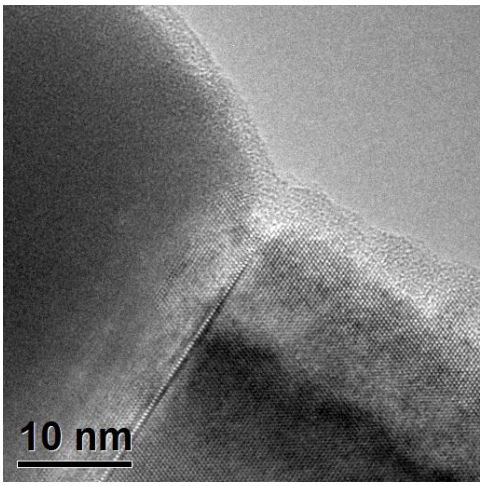


**Figure 9.** TEM image of Si on GaAs heterostructure nanowire grown by Ga-assisted VLS

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